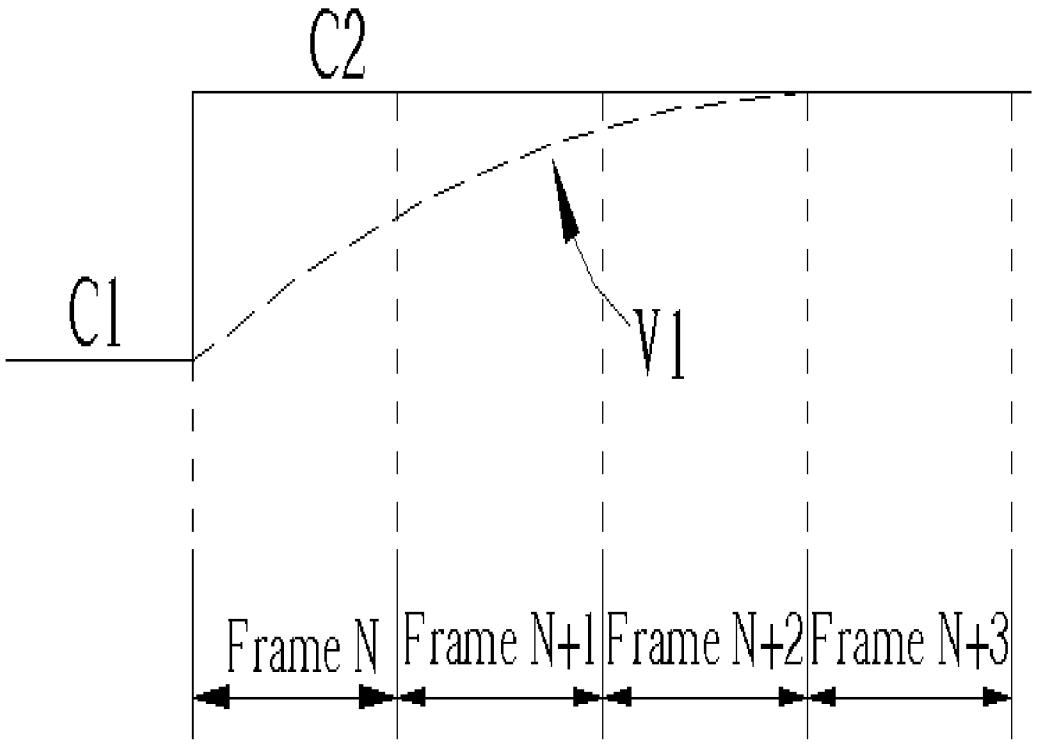


Fig. 1 Prior art

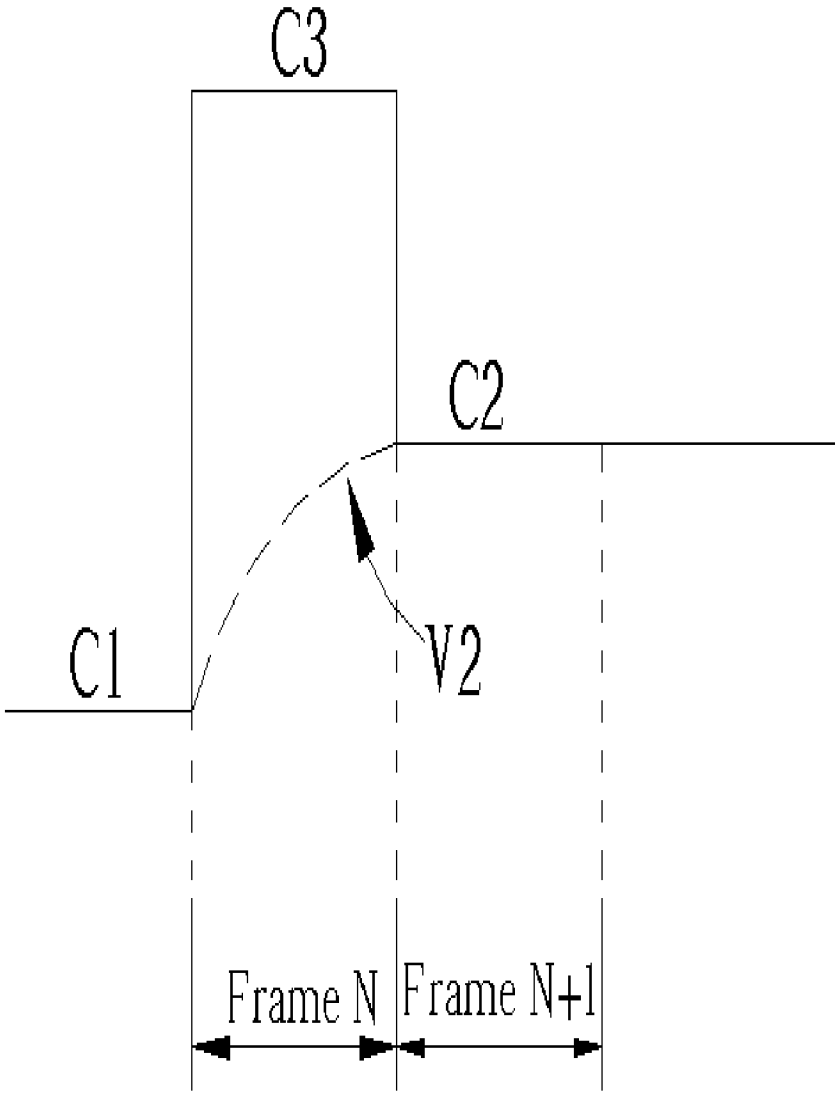


Fig. 2 Prior art

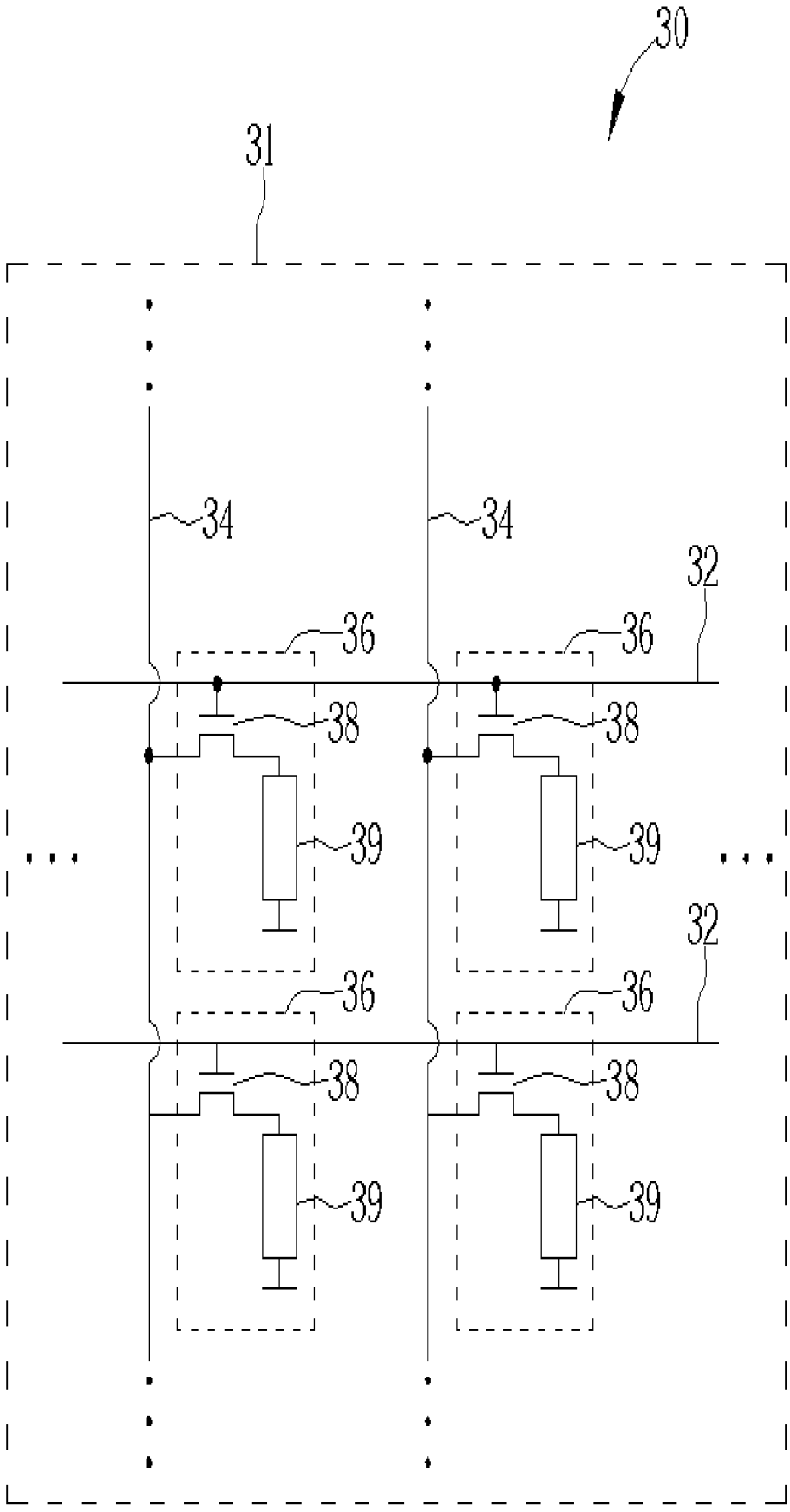


Fig. 3 Prior art

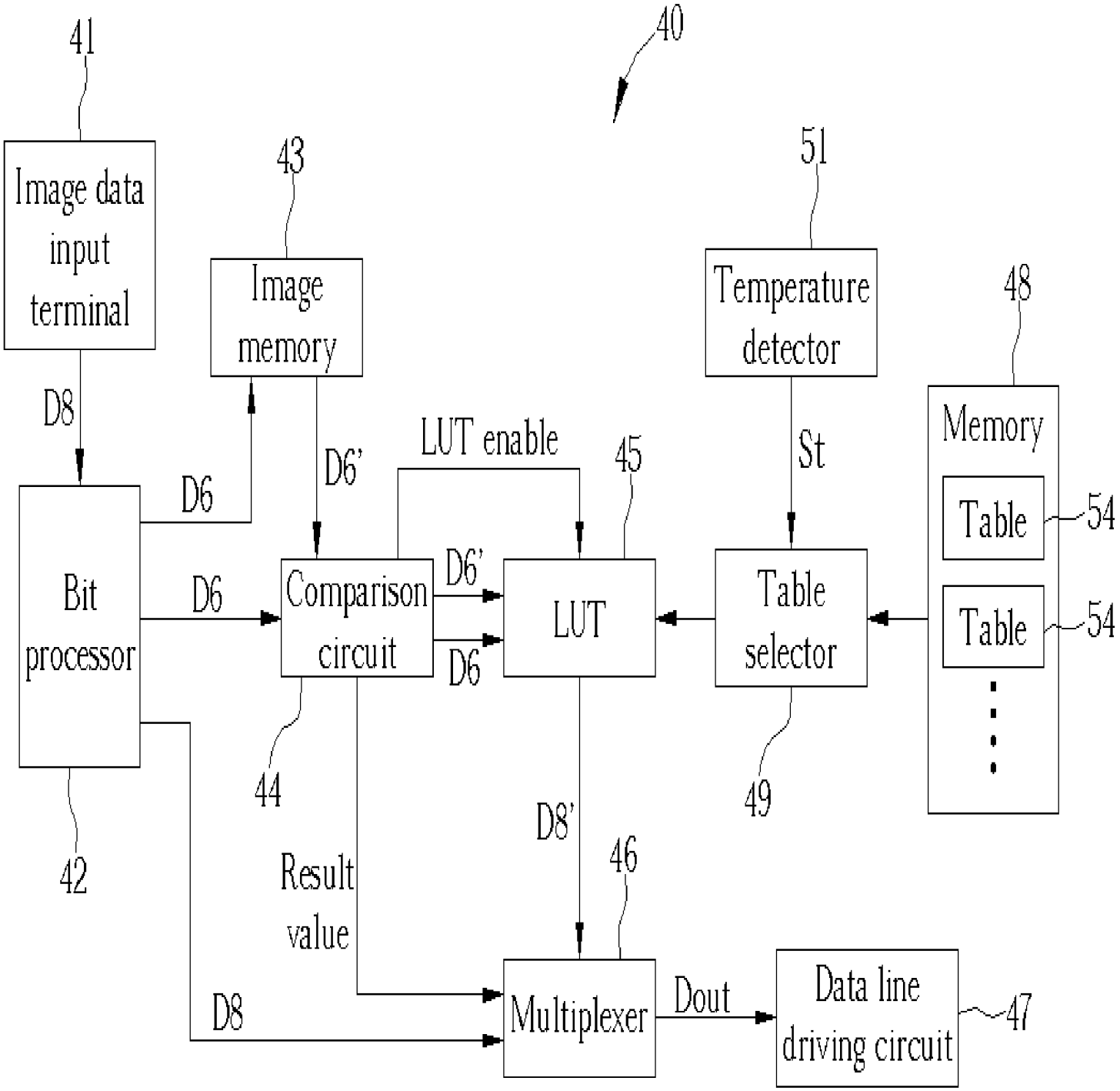

41
40
Image data input terminal
43
Image memory
51
Temperature detector
48
Memory
D8
D6
D6'
LUT enable
45
St
Table
54
Bit processor
D6
Comparison circuit
D6'
D6
LUT
Table selector
Table
54
44
49
42
D8'
46
Result value
D8
Multiplexer
Dout
Data line driving circuit
47

Fig. 4

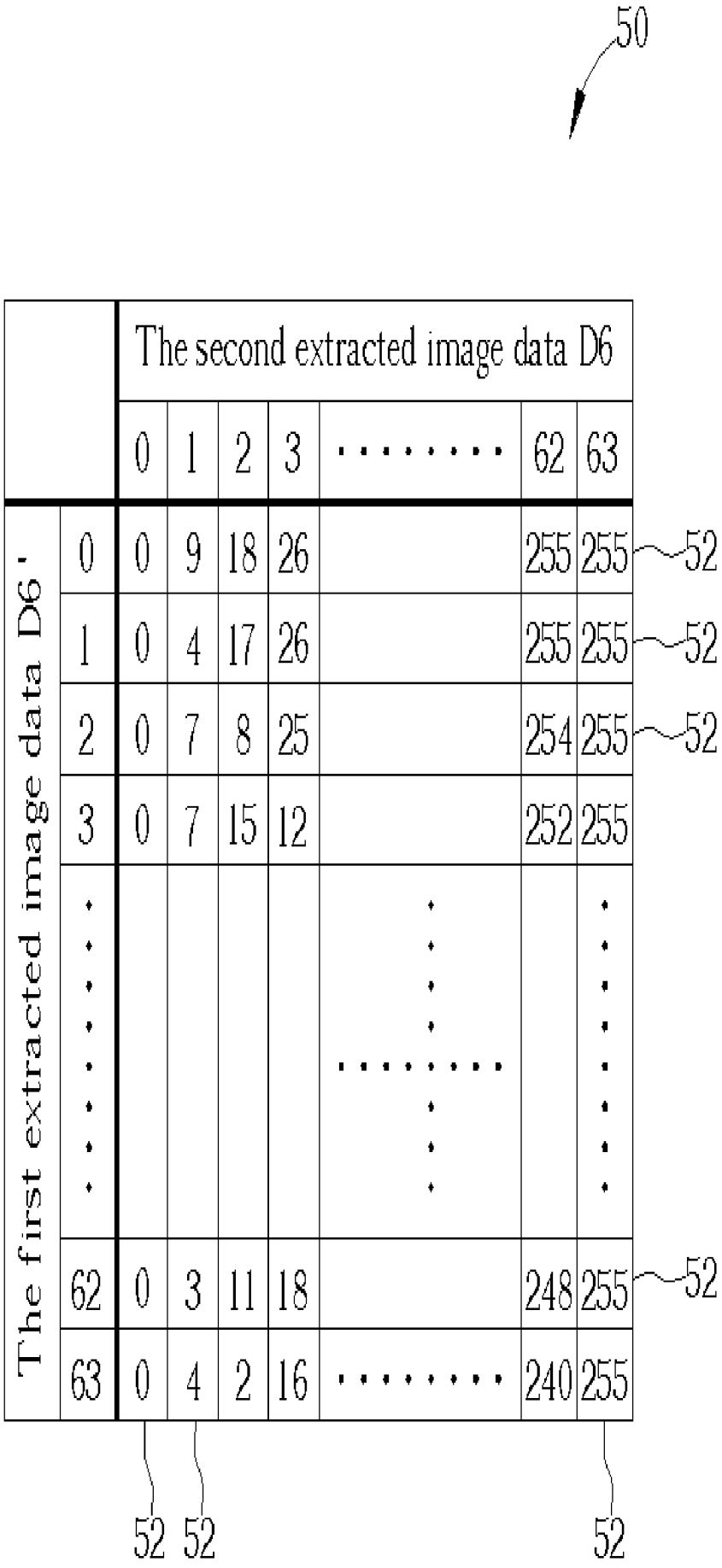

50
The second extracted image data D6
0 1 2 3 ..... 62 63
The first extracted image data D6'
0 0 9 18 26 255 255 52
1 0 4 17 26 255 255 52
2 0 7 8 25 254 255 52
3 0 7 15 12 252 255
62 0 3 11 18 248 255 52
63 0 4 2 16 240 255
52 52 52

Fig. 5

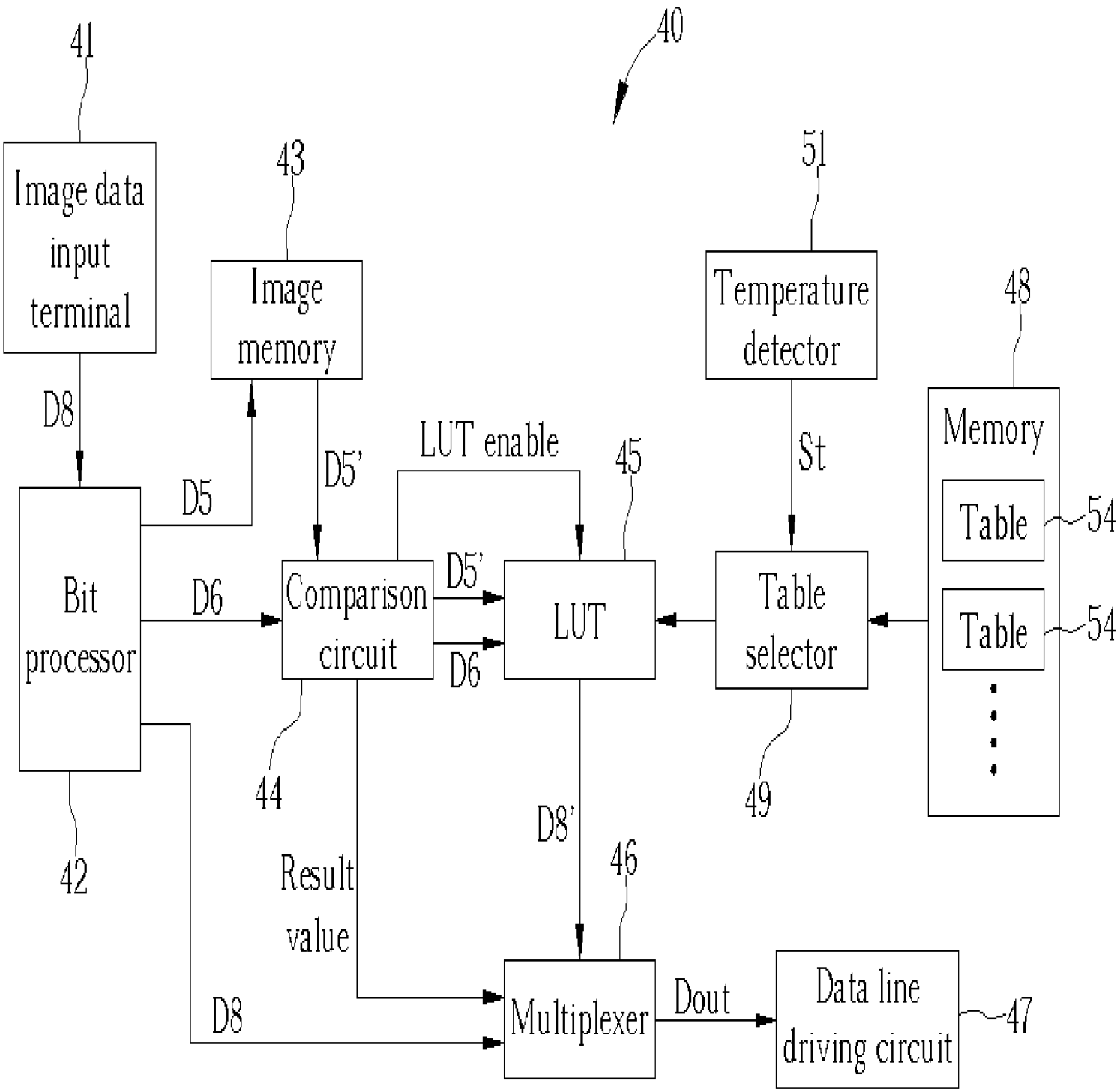
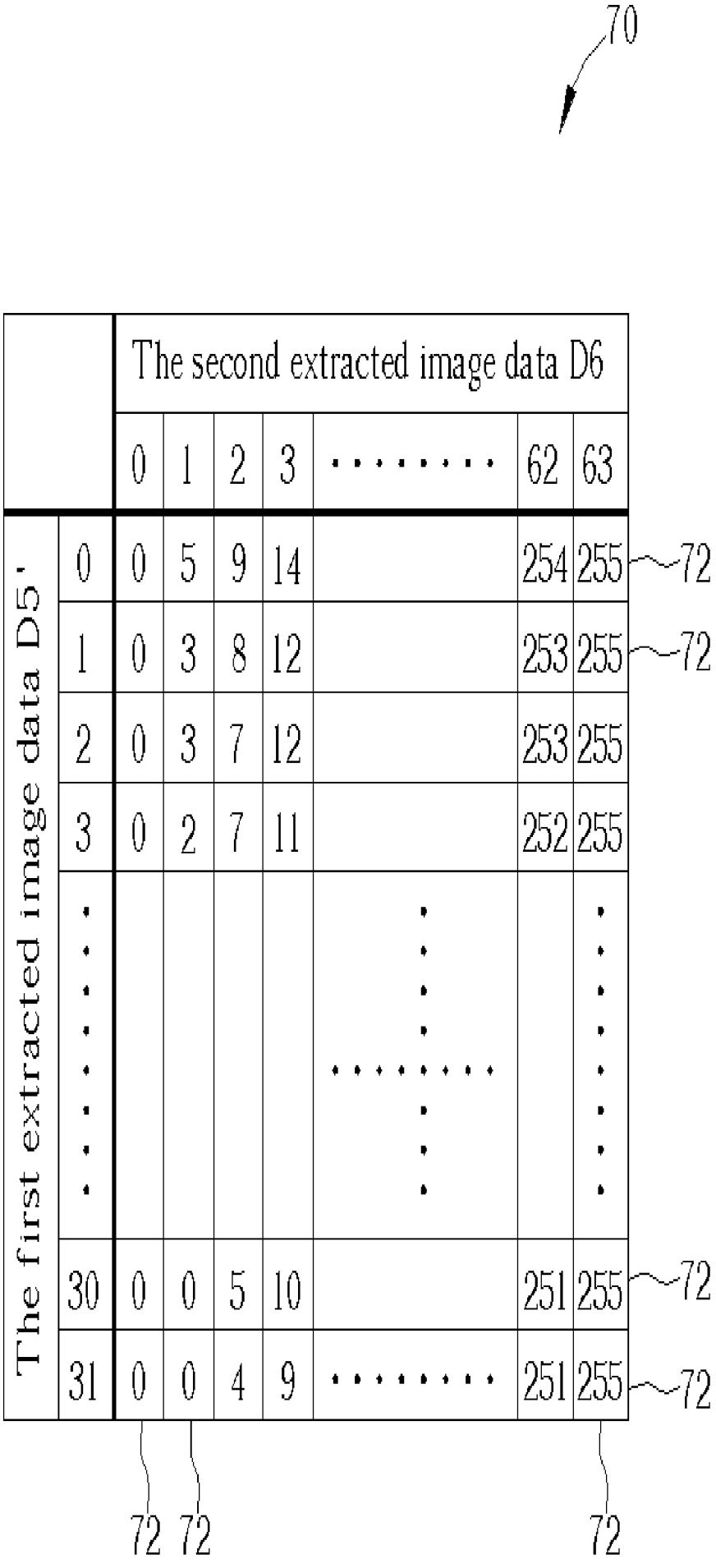

40
41
Image data input terminal
43
Image memory
51
Temperature detector
48
Memory
Table
54
Table
54
D8
D5
D5'
LUT enable
45
St
Bit processor
D6
Comparison circuit
D5'
D6
LUT
Table selector
44
49
42
D8'
46
Result value
D8
Multiplexer
Dout
Data line driving circuit
47

Fig. 6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The second extracted image data D6
0 1 2 3 ..... 62 63
The first extracted image data D5'
0 0 5 9 14 ..... 254 255 72
1 0 3 8 12 ..... 253 255 72
2 0 3 7 12 ..... 253 255
3 0 2 7 11 ..... 252 255
30 0 0 5 10 ..... 251 255 72
31 0 0 4 9 ..... 251 255 72
72 72 72

Fig. 7

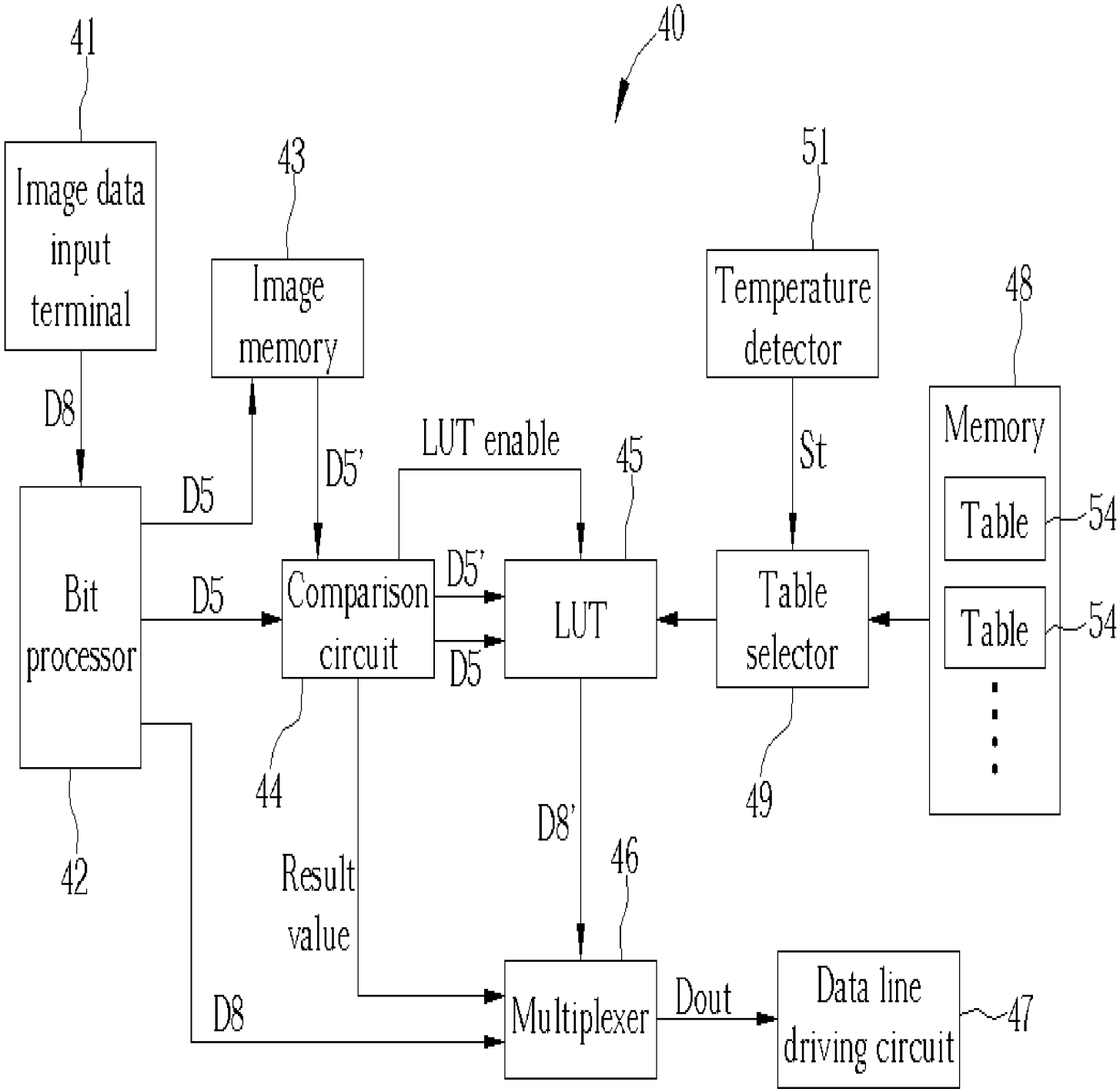
41
40
Image data input terminal
43
Image memory
51
Temperature detector
48
Memory
D8
D5
D5'
LUT enable
45
St
Table
54
Bit processor
D5
Comparison circuit
D5'
D5
LUT
Table selector
Table
54
44
49
42
D8'
46
Result value
D8
Multiplexer
Dout
Data line driving circuit
47

Fig. 8

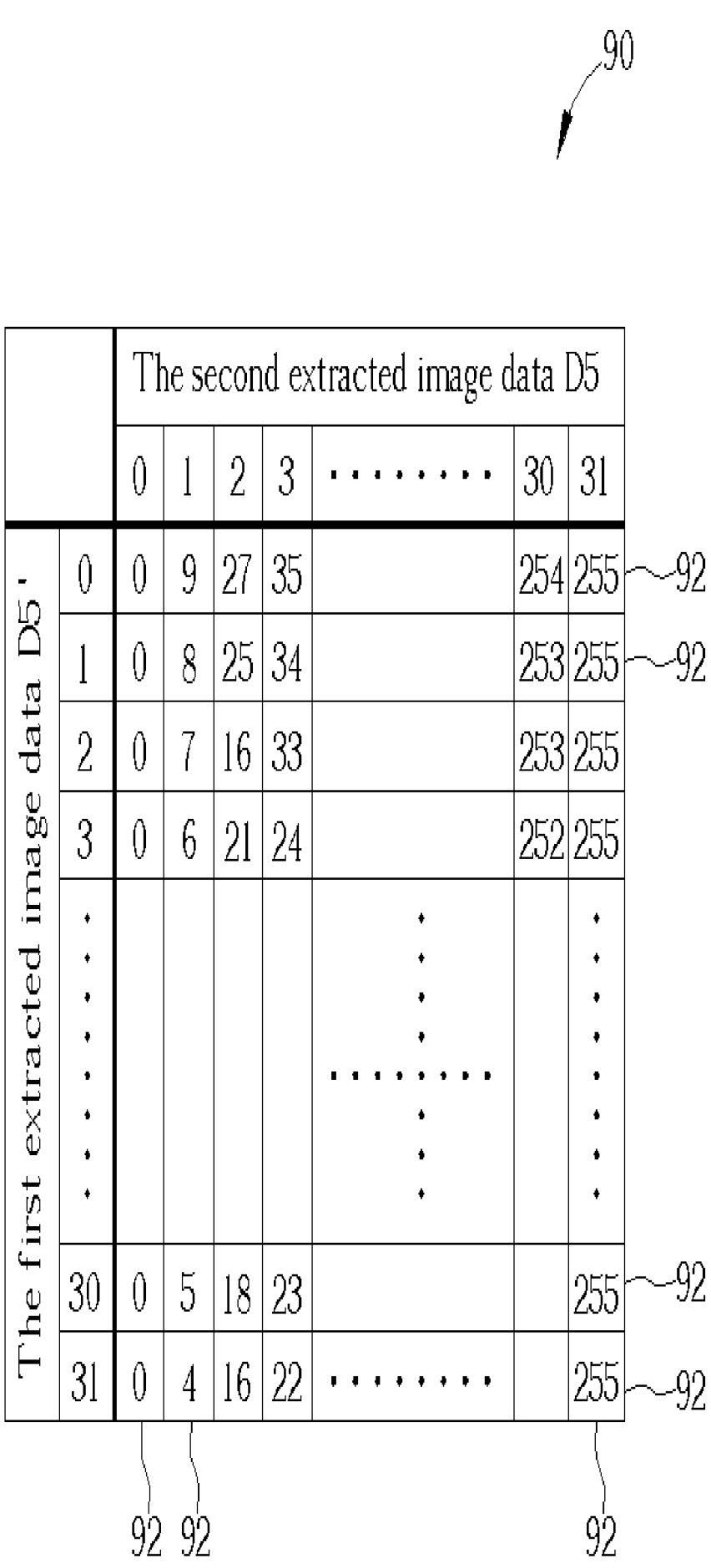
90
The second extracted image data D5
0 1 2 3 ..... 30 31
The first extracted image data D5'
0 0 9 27 35 254 255 92
1 0 8 25 34 253 255 92
2 0 7 16 33 253 255
3 0 6 21 24 252 255
30 0 5 18 23 255 92
31 0 4 16 22 255 92
92 92 92

Fig. 9

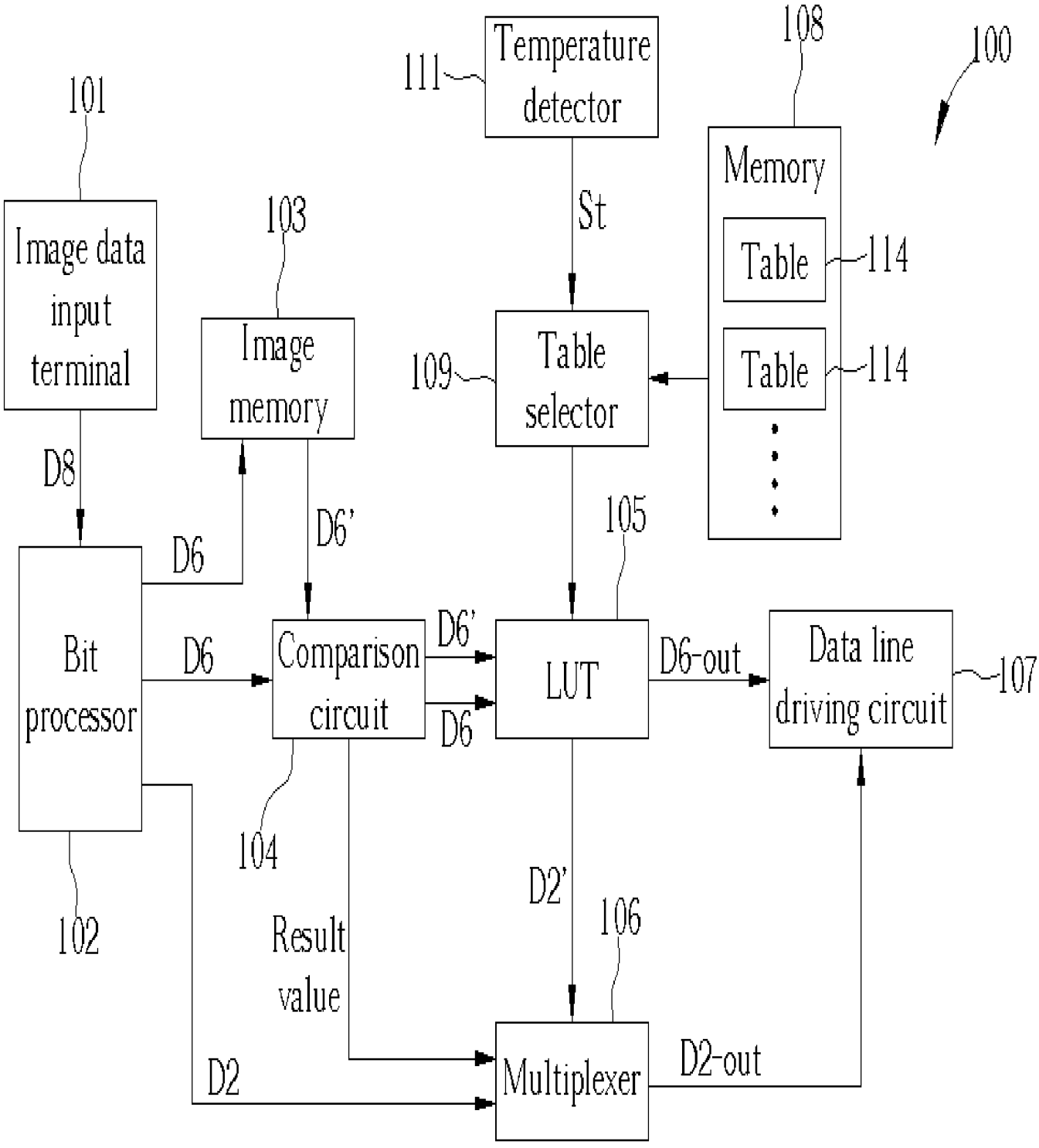
100
101
Image data input terminal
102
103
Image memory
104
105
106
107
108
Memory
Table
Table
114
114
109
Table selector
111
Temperature detector
St
D8
D6
D6'
Bit processor
Comparison circuit
D6
D6'
LUT
D6-out
Data line driving circuit
D2'
Result value
D2
Multiplexer
D2-out

Fig. 10